REMARKS

Claim Rejections - 35 U.S.C. § 102/103

The Examiner has rejected claims 1-4, 6-8 and 10 under 35 U.S.C. § 102(e) as being anticipated by Lin (U.S. Patent 6,297,554). Claims 5, 9 and 24 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lin (U.S. Patent 6,297,554) in view of Cho et al. (U.S. Patent 6,140,252).

It is Applicant's understanding that the cited references fail to teach or render obvious Applicant invention as claimed in claims 1-9 and 24.

With respect to an independent claim 1, Applicant teaches and claims a process of lowering a parasitic capacitance between interconnect lines by forming a first dielectric layer and patterning the first dielectric layer such that a plurality of vertically oriented posts are formed, with each post having a top surface. The first dielectric layer has a dielectric constant. The process further comprises the formation of a second dielectric layer over and adjacent to the posts, where the second dielectric layer has a top surface and substantially fills out the area adjacent to the posts. The second dielectric layer has a constant than is lower than the constant of the first dielectric layer. The above mentioned posts are formed to provide a mechanical reinforcement of the bulk of the inter-layer dielectric material. Finally, the process comprises the polishment of the second dielectric layer such that its top surface is substantially even with the top surfaces of the posts and the formation of an inlaid metal interconnection in the second dielectric layer.

On the other hand, Lin discloses a process of reducing the effective dielectric constant due to the trenches 72 in the dielectric layer 60 and the voids formed in the trenches 72. (See Fig. 2, 3).

The process disclosed in Lin comprises a silicon substrate covered by a dielectric layer 52, a plurality of metallic conductors 61 in the dielectric layer 52, a silicon nitride layer 54 covering the dielectric layer 52, and a stacked dielectric layer 62 covering the silicon nitride layer 54. The patterns of the via holes 63, 64 and trenches 71 have been defined in a photoresist layer 42 over the stacked dielectric layer 62 using a conventional lithographic process. The staked dielectric layer 62 comprises a silicon oxide layer 56, an etching stop layer 58 covering the silicon oxide layer, and a dielectric layer 60 covering the etching stop layer. (See Fig. 1)

Next, Lin discloses a dry etching process that is performed to transfer the patterns of the via holes 63, 64 and the trenches 71 in the photoresist layer 42 to the dielectric layer 60. (See Fig. 2)

Further, as shown in Fig. 3, another CVD process is performed to uniformly deposit an insulating layer 82 on the surface of the dielectric layer 60, the surface of the via hole patterns 65, 66, and the surface of the trenches 72. The insulating layer 82 is composed of low-dielectric constant materials. The insulating layer 82 forms overhangs on the dielectric layer 60 around the top edges of the opening of the trenches 72, and these overhangs close the trenches so as to form the voids 73.

Next, as shown in Fig. 4, Lin discloses an RCA standard cleaning procedure that is performed on the surface of the semiconductor wafer 40 and a dehydration process is used to dry the surface of the semiconductor wafer 40. Then, a positive type photoresis layer 44 is coated on the surface of the semiconductor wafer 40. A lithographic process is used to define trench patterns 43 of the copper wiring lines 91, 92, 93.

Further, as shown in Fig. 5, Lin discloses a reactive ion etching process with fluoroform as a reactive gas which is performed to vertically remove the portion of the insulating layer 82 and the dielectric layer 60 that are not covered by the photo resist layer 44 down to the surface of the etching stop layer 58. The trench pattern 43

is thus transferred to the dielectric layer 60 to form new trench pattern 67, 68, 69 in the dielectric layer 60. The via hole patterns 65, 66 are also transferred to the etching stop layer and the silicon oxide layer 56 so as to expose the copper conductors 61.

Next, as shown in Fig. 6, Lin discloses a performance of a deposition process of copper layer 84. As a result, a barrier layer 90 is usually formed before deposition of the copper layer 84.

Finally, as shown in Fig. 7, a global planarization process, such a chemical mechanical polishing (CMP) process, is then performed to remove the copper layer 84 down to the surface of the insulating layer 82 so as to form the copper wire lines 91, 92, 93.

The process of reducing the effective dielectric constant described in Lin is different from the process of reducing a parasitic capacitance disclosed in the presently claimed invention. First of all, in the presently claimed invention, a second dielectric layer is formed over and adjacent to the post and fills up substantially the whole area adjacent to the posts. The dielectric constant of the first dielectric layer is higher than the dielectric constant of the second dielectric layer. The second dielectric layer makes up the bulk of the inter-layer dielectric material. In Lin, the insulating layer 82 is uniformly deposited on the surface of the dielectric layer 60, the surface of the via hole patterns 65, 66, and the surface of the trenches 72. The insulating layer 82 forms overhangs on the dielectric layer 60 around the top edges of the opening of the trenches 72, and these overhangs close the trenches so as to form the voids 73. (See Fig. 3) Thus, in Lin insulating layer 82 does not form the bulk of the inner-layer dielectric material due to a serving purpose of forming voids 73 by closing trenches 72, rather dielectric layer 60, with higher dielectric constant than insulating layer 82, forms the bulk of the inner-layer dielectric material. In the presently claimed invention, in contrast, the second dielectric layer, with the

dielectric constant lower than the first layer, forms the bulk of the inner-layer dielectric material.

Further, in Lin the trench structure of the dielectric layer 60 and the insulating layer 82 that closes the trenches of the dielectric layer 60 are only created for the purpose of forming a plurality of voids. In the present invention, the first dielectric layer is used to form a plurality of vertically oriented posts, which are used to provide mechanical reinforcement to the comparative weak highly porous, low-k dielectric material, which forms the second dielectric layer. Further, in the present invention, posts provide the mechanical strength and stability to withstand the forces encountered during processing steps such as chemical mechanical polishing. Thus, the posts in the Lin are not used to provide mechanical reinforcement as do the posts in the presently claimed invention.

Finally, in Lin global planarization process, such as a chemical mechanical polishing (CMP) process is performed to remove the copper layer 84 down to the surface of the insulating layer 82 so as to form the copper wiring lines 91, 92, 93. (See Fig. 7) CMP process in Lin is the last step in the process of forming a structure of a dielectric layer between two adjacent copper wiring lines. (Fig.1 – 8) In the presently claimed invention the formation of inlaid metal interconnection in the second dielectric layer takes place after CMP process. Thus, in Lin the formation of inlaid metal interconnection does not take place after CPM as it takes place in the presently claimed invention.

Thus, Lin does not teach or suggest the second dielectric layer that makes up the bulk of the inter-layer dielectric material having the dielectric constant lower than the first dielectric layer, posts that provide a reinforcement structure, and formation of the inlaid interconnection in the second dielectric layer after the CMP process.

Furthermore, Cho lacks at least the elements missing from Lin.

Thus, Lin and Cho, taken alone or in combination, do not teach or suggest the presently claimed invention. Therefore, applicant request withdrawal of 102(e) and 103(a) rejections and submits that claims 1-9 and 24 are in condition for allowance.

Deposit Account Authorization

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due. Furthermore, if an extension is required, then Applicant hereby requests such extension.

If the Examiner determines the prompt allowance of these claims could be facilitated by a telephone conference, the Examiner is invited to contact Michael A. Bernadicou at (408) 720-8300.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A process, comprising:

forming a first dielectric layer on a substrate, wherein the first dielectric layer has a dielectric constant;

patterning the first dielectric layer such that a plurality of vertically oriented posts are formed, the post having a top surface;

forming a second dielectric layer over and adjacent to the posts, the second dielectric layer having a top surface and substantially filling up the area adjacent to said posts, wherein the second dielectric layer has a dielectric constant, said dielectric constant of the first layer being higher than said dielectric constant of the second layer;

wherein said plurality of vertically oriented posts are used to provide mechanical reinforcement of the second dielectric layer which makes up the bulk of an inter-layer dielectric material;

polishing the second dielectric layer such that its top surface is substantially even with the top surfaces of the posts; and

forming an inlaid metal interconnection in the second dielectric layer.

24. (Amended) A process, comprising:

depositing a silicon nitride layer on a wafer;

depositing an insulating layer over the silicon nitride layer, wherein the insulating layer has a dielectric constant;

patterning the insulating layer such that a plurality of structures are formed, the structures each having a top surface;

depositing a porous dielectric material over and adjacent to the structures, the porous dielectric material having a void fraction, <u>wherein the porous dielectric material substantially fills out the area adjacent to said structures and wherein the porous dielectric material has a dielectric constant, said dielectric constant of the insulating layer being higher than the dielectric constant of the porous dielectric material;</u>

<u>wherein said plurality of structures formed in the insulating layer provides mechanical reinforcement of the porous dielectric material which makes up the bulk of an inter-layer dielectric material;</u>

polishing the porous dielectric material such that a top surface thereof is substantially even with the top surfaces of the structures;

treating the porous dielectric material such that its void fraction is increased; and

<u>forming an inlaid metal interconnection in the porous dielectric material.</u>